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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Rolf E. Carlson

Serial No.: 08/959,575

Filed: October 28, 1997

For: **SYSTEM FOR GENERATING
RANDOM NUMBERS USING A
UNIVERSAL GAMING ENGINE
(AS AMENDED)**

Art Unit: 2767

Examiner: D. Meislahn

Docket No.: 1505/5(a)

AMENDMENT UNDER 37 C.F.R. §1.111

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

DEAR SIR:

In the communication dated July 8, 1999, Claims 17-22 and 29-43 were rejected. Applicant has amended the title and Applicant has amended Claims 17, 33, 39, 40 and 42-43 to more particularly point out and distinctly claim the invention. Reconsideration of the application, as amended, is respectfully requested.

In the Specification:

Please change the title to read: -- SYSTEM FOR GENERATING RANDOM NUMBERS USING A UNIVERSAL GAMING ENGINE --.

In the Claims:

SUB-D-17
C 1
17. (Twice Amended) A random number generator comprising:
a controller;
at least one random number circuit connected to said controller, said at least one random number circuit [providing] generating a series of pseudo-

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C 1
Cont'd

5 random numbers and providing said series of pseudo-random numbers to said controller, said series of pseudo-random numbers comprising a plurality of raw pseudo-random numbers wherein each of said plurality of raw pseudo-random numbers are stored by said controller; and

10 a verifier connected to said controller, said verifier receiving said stored raw pseudo-random numbers from said controller, said verifier verifying that each of said plurality of raw pseudo-random numbers is statistically random, said verifier supplying a series of statistically verified pseudo-random numbers, said series of statistically verified pseudo-random number being provided continuously.

15

33. (Amended) A random number generator comprising:

a controller;

a random number generator connected to said controller, said random number generator [providing] generating a series of random numbers and providing said series of random numbers to said controller, said series of random numbers comprising a plurality of raw random numbers wherein each of said plurality of raw random numbers are stored by said controller; and

10 a verifier connected to said controller, said verifier receiving said stored raw random numbers from said controller, said verifier supplying a series of statistically verified random numbers, said series of statistically verified random numbers being provided continuously.

C 2

39. (Amended) The random number generator of claim 33 further comprising:

an encryption circuit connected to said random number generator, said encryption circuit encrypting said series of random numbers and supplying said 5 series of encrypted random numbers to said controller.

C 3
cont

40. (Amended) The random number generator of claim 33 further comprises:

a plurality of encryption standard (DES) circuits connected to said random number generator, said plurality of encryption circuits encrypting said series of pseudo-random numbers and supplying said series of encrypted pseudo random-numbers to said controller.

C 4

42. (Amended) A random number generator comprising:

a controller;

at least one random number circuit connected to said controller, said at least one random number circuit [providing] generating a series of pseudo-random numbers and providing said series of pseudo-random numbers to said controller, said series of pseudo-random numbers comprising a plurality of raw pseudo-random numbers wherein each of said plurality of raw pseudo-random numbers are stored by said controller;

a verifier connected to said controller, said verifier receiving said stored raw pseudo-random numbers from said controller, said verifier verifying that each of said plurality of raw pseudo-random numbers is statistically random, said verifier supplying a series of verified pseudo-random numbers, said series of statistically verified random numbers being provided continuously;

a buffer having an output, said buffer receiving said series of statistically verified pseudo-random numbers, said buffer providing said series of statistically verified pseudo-random numbers to said output,

wherein said buffer receives said series of statistically verified pseudo-random numbers at a first rate, said buffer supplying said series statistically verified pseudo-random numbers to said output at a second rate, said first rate greater than said second rate, said buffer providing short-term bursts of said series of statistically verified pseudo-random numbers to said output during said short-term bursts said second rate is greater than said first rate.

*C4
Cn't*

43. (Amended) A random number generation system comprising:
a verifier;
a random number generator connected to said verifier, said random
number generator [supplying] generating a series of random numbers and
supplying said series of random numbers to said verifier, said series of random
numbers comprising a plurality of raw random numbers,
said verifier verifying that each of said raw random numbers is
statistically random, said verifier supplying a series of statistically verified
random numbers, said series of statistically verified random numbers being
provided continuously.

REMARKS

Applicant has amended the title. In addition, Applicant has amended Claims 17, 33, 39, 40 and 42-43 to more particularly point out and distinctly claim the invention. Reexamination and reconsideration of the application, as amended, is respectfully requested. In view of the amendments and argument presented below, Applicant respectfully requests that the rejection of Claims 17-22 and 29-43 be withdrawn and that the application be fully allowed.

A. Title Amendment

The title has been objected to as being non-descriptive of the present invention. Applicant has amended the title to recite a System For Generating Random Numbers Using A Universal Gaming Engine. Applicant believes that this amendment makes the title clearly descriptive of the present invention to which the claims are directed.

B. Claim Amendments

Applicant has amended Claims 17, 33, 39, 40 and 42-43 to more particularly point out and distinctly claim the present invention. Support for the amended claim language can be found on page 14, lines 25-32; page 15, lines

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1-5 and page 16, lines 25-32 of the specification. Based on these amendments, the present invention is patentable over the Vasseur I, Vasseur II and Murata references, alone or in combination, and full allowance is requested.

Independent Claims 17, 33, 42 and 43 have been amended to recite that the random number generator circuit generates a series of random numbers and provides the series of random number to the controller. In addition, independent Claims 17, 33, 42 and 43 have been amended to recite that the series of statistically verified random number are provided continuously. This amended language particularly points out that it is the random number generator circuit that generates and supplies the series of random number to the controller, and that the verifier continuously provides the statistically verified random numbers even when non-random numbers are generated. Claims 39 and 40 have been made to clearly point out that it is the series of random numbers that is encrypted into the series of encrypted random numbers. Therefore, based on these amendments the present invention is patentable over Vasseur I, Vasseur II and Murata, alone or in combination.

C. Rejections and Arguments

1. Rejection of Claims 17, 30, 33, 34 and 43 under 35 U.S.C. §102

Claims 17, 30, 33 34 and 43 have been rejected under 35 U.S.C. §102 as being anticipated by Vasseur (U.S. Patent No. 3,309,509) (hereinafter termed Vasseur I). The rejection states that Vasseur I shows a key generator that produces random numbers (Fig. 2). In addition, the rejection states that, although Vasseur I does not expressly state the storage and controller distribution of keys, such operation is inherent to key generation. Also, the

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rejection further states that the decoder, shown in Fig. 2, can be used as an encryption circuit.

In the present invention, as claimed in independent Claims 17, 33 and 43 a random number generator circuit generates a series of random numbers. The series of random numbers is provided to a controller where the random numbers are statistically verified by a verifier.

For the following reasons, it is maintained that Vasseur I is not an anticipatory reference: (1) Vasseur I checks only the key generation (i.e., letters and symbols) and not the random number generation. (2) Vasseur I generates an alarm and/or stops the machine when an anomaly is detected (col. 2, lines 57-60); (col. 3, lines 11-13 and lines 36-37) and (col. 4, lines 1-3). (3) Vasseur I does not teach, suggest or imply storage and distribution of random number, nor is it inherent.

First, the Vasseur I reference discloses a key generator that "delivers to its output wires b_1 and b_5 one of 32 letters" (col. 1, lines 54-57) (emphasis added). As such, Vasseur I discloses a key generator that generates letters which are used as key values and which are limited to 32 letters provided over 5 lines. Therefore, the Vasseur I device is limited to a precise number such as a collection of 32 possible random letters or symbols.

The present invention claims a random number generator circuit that generates a series of random numbers and a verifier that statistically verifies the random numbers. In addition, the present invention provides no limit on the size of the random numbers produced by the random number circuit. In contrast, the Vasseur I device provides only a precise number such as 32 possible random letters or symbols. As such, Vasseur I does not disclose a device with sufficient resolution to be used with the present invention. Therefore, Vasseur I does not teach or disclose a random number generator circuit that generates a series of random events that can be used with the

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present invention. In fact, the present invention would not be useful if it were used with the Vasseur I device because Vasseur I provides for the verification of only 32 possible random letters or symbols. Therefore, the present invention is not anticipated under §102 by Vasseur I.

The possibility that the key values recited in Vasseur I may be used to generate random numbers has no effect because Vasseur I does not teach or disclose the verification of the random number to ensure that the series is statistically random, and the Vasseur I reference provides an upper limit to the output from the key generator. In addition, such a possibility is mere speculation because Vasseur I does not teach or disclose the generation of a series of random numbers. Therefore, since Vasseur I does not teach or disclose the generation of random numbers or the statistical verification of the randomness of the random numbers, the present invention as claimed in independent Claims 17, 34 and 42 and their dependent claims is not anticipated by the Vasseur I reference.

Second, independent Claims 17, 33 and 43 claim a verifier that not only statistically verifies that the series of random numbers is statistically random, but supplies a continuous series of statistically verified random numbers. Vasseur I only "checks" for an anomalous discrepancy and then stops the machine and/or raises an alarm when such an anomaly is detected. This stopping and/or alarm activation does not occur in the claimed invention as amended. The claimed invention continuously provides verified random numbers even when a non-random series of numbers are generated (see page 16, lines 25-32). "Anticipation requires that the disclosure in a single prior art reference of each element of the claim under consideration." W.L. Gore & Assoc. v. Garlock, 220 USPQ 303, 313 (Fed. Cir. 1983) (emphasis added). The rejection of independent Claims 17, 33 and 43 does not set forth an element in the Vasseur I that is equivalent to the verifier of the present

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invention, and in addition a verifier that continuously proves a series of statistically verified random numbers. As such, a *prima facie* case of anticipation has not been established. Therefore, the present invention cannot be anticipated by the Vasseur I reference.

Further, the rejection states that Vasseur I does not recite the storage and controlled distribution of the keys, but such storage and distribution is inherent to key generation. The Federal Circuit has stated that inherency "may not be established by probability or possibility. The mere fact that a certain thing may result from a given set of circumstances is not sufficient [for inherency]." Continental Can Co. USA v. Monsanto Co., 20 USPQ2d 1746, 1749 (Fed. Cir. 1991) (emphasis added). As such, the missing element (the controller) that stores and distributes the random numbers must necessarily be disclosed or implied from the teaching in Vasseur I. However, the teaching in Vasseur I does not necessarily provide a controller that stores and distributes random numbers. As stated above, the Vasseur I reference does not teach or suggest the generation of random numbers or a device that stores or distributes random numbers. Therefore, it cannot be suggested that storing and distribution of random number necessarily flows from the disclosure of Vasseur I when Vasseur I does not teach or disclose the generation of a series of random numbers. As such, the present invention, as claimed in Claims 17, 30, 33-34 and 43 is not anticipated by Vasseur I.

In addition, with regard to Claim 30, the rejection states that the Vasseur I reference discloses a decoder that can be used by an encryption circuit. Claim 30 claims that the random number generator circuit comprises at least one encryption circuit. The Vasseur I reference does not teach or disclose that the decoder is used to generate a series of random numbers as part of a random number generator circuit. In contrast, the decoder of Vasseur I outputs a signal corresponding to the outputs b_1 and b_5 from the key

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generator (col. 1, lines 54-72), and as stated previously, Vasseur I does not teach or disclose that the key generator produces or generates random numbers. Therefore, the Vasseur I reference does not teach or suggest that the decoder is used with a random number generator circuit to generate random numbers and to provide a continuous series of statistically verified random numbers. Therefore, Claim 30 is not anticipated by the Vasseur I reference.

Based on the amendments and the arguments presented above, the present invention, as claimed in Claims 17, 30, 33-34 and 42, is not anticipated by the Vasseur I reference. Therefore, the rejection under 35 U.S.C. §102 should be withdrawn.

2. Rejection of Claims 18-22, 29-32 and 35-42 under 35 U.S.C. §103

Claims 18-22, 29-32 and 35-42 have been rejected under 35 U.S.C. §103 as being unpatentable over Vasseur I, alone or in combination with Vasseur (U.S. Patent No. 4,179,663) (hereinafter termed Vasseur II) or Murata (U.S. Patent No. 5,361,323). Each of the rejection is specifically set out below. For all of the reasons articulated above, the present invention is patentably distinct over Vasseur I.

a. Claims 18 and 36 rejected over Vasseur I and Murata

Claims 18 and 36 have been rejected as being unpatentable over Vasseur I and Murata. The rejection states that Vasseur I teaches a random number generation and a verification circuit, but does not disclose a buffer storing numbers. The rejection further states that Murata discloses outputting pseudo-random numbers that have been stored in a buffer.

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In Claims 18 and 36, a buffer is provided having an output. The buffer receives a series of statistically verified random numbers and provides the statistically verified random numbers to an output.

The Vasseur I reference has been set forth above and that discussion is incorporated in this section. Vasseur I relates, generally, to a key generator. The Murata reference relates to a signal encoding device. As pointed out in the rejection, the Murata reference discloses that "a code output circuit 34 outputs the initial values of the pseudo-random number generator stored in the second buffer 31" (col. 18, lines 16-18). If Vasseur I generates random keys and then stops when an anomaly exists, then Murata cannot store in its buffer any further random keys. Alternatively, if Vasseur I continues to generate random keys and raises an alarm when an anomaly is present, then Murata stores some keys that are anomalous. In any event, the combination of Vasseur I and Murata does not meet the limitations of the claimed invention.

The Murata reference further discloses that "the initial value set in the pseudo-random number generator 24 for the pattern that provides the distance of the minimum value E_{min} and the gain adjustment amount by the gain controller 27 for the pattern are sent to a second buffer 34" (col. 17, lines 34-39). Murata further discloses that "[w]hen the distance E_m has been calculated, the pseudo-random number sends out the next pattern through the digital filter 25 into the pattern shift register 23b" (col. 17, lines 20-24). As shown in Figs. 15 and 17 of Murata, the flow of these patterns bypass the buffer 34 and are not stored.

As such, the Murata reference discloses that an "initial value set" is sent from the pseudo-random number generator 24 to the second buffer 31. This "initial value set" is not necessarily stored as a series of verified random numbers, as claimed in Claims 18 and 36. Further, the Murata device stores an "initial value set" from a series of patterns output from the pseudo-random



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number generator 24, and Murata does not teach or suggest that this "initial value set" comprises verified random numbers as claimed in Claims 18 and 36. Therefore, since Murata does not teach or suggest the storage of a series of verified random numbers in the buffer, Murata does not meet the limitations of the claimed invention. Thus, the combination of Vasseur I and Murata does not produce a resultant structure that meets the limitations of the claimed invention, and, as such, the rejection is improper.

In addition, no suggestion can be found in either Vasseur I or Murata to make the combination stated in the rejection. "Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination."

In re Fritch, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992). In this regard, Vasseur I and Murata make no suggestion or indication that the respective devices are used to process random numbers or verified random numbers. Therefore, the combination of Vasseur I and Murata is improper.

Furthermore, since there is not motivation or suggestion to make the combination stated in the rejection, the present rejection is based on impermissible hindsight. The Federal Circuit has stated that "[i]t is impermissible to use the claimed invention as an instruction manual or "template" to piece together teachings of the prior art so that the claimed invention is rendered obvious . . . one cannot use hindsight reconsideration to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." In re Fritch, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992). Therefore, since there is no motivation or suggestion to make the combination suggested in the rejection, the rejection is based on improper hindsight construction and the rejection under 35 U.S.C. §103 is improper.

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Based on these amendments and arguments presented, Claims 18 and 36 are not obvious over the combination of Vasseur I over Murata. As such, the rejection under 35 U.S.C. §103 should be withdrawn.

b. Claim 20 rejected over Vasseur I and Vasseur II

Claim 20 has been rejected under 35 U.S.C. §103 as being unpatentable over Vasseur I and Vasseur II. The rejection states that Vasseur I teaches random number generation and a verification circuit, but Vasseur I does not disclose using two random number generators. The rejection further states that Vasseur II teaches a system using two sequence generators.

In Claim 20, at least two random number generator circuits are provided that each have independent seed and key values. The random number generator circuits provide at least two independent series of random numbers. The controller couples to the random number generator circuits to receive each of the series of random numbers.

The Vasseur I reference has been set out above and that discussion is incorporated in this section. Vasseur I discloses a key generator. The Vasseur II reference relates to a device for generating pseudo-random sequences. The Vasseur II reference discloses a “[first] generator device producing a pseudo-random sequence S_1 , whose output is connected . . . to first input 20 of electronic switch 13, and . . . to the second input of said switch via a level inverter 12[, and] . . . [t]he switch has a single output 23 and a control input 22 connected to the output of a [second] generator 14 producing a pseudo-random sequence of S_c of binary control digits” (col. 2, lines 57-66).

Vasseur II teaches a first generator that produces one series of random numbers and a second generator that produces binary control digits. Vasseur II does not teach or suggest a least one random number generator circuit that connects to a controller. Further, Vasseur does not teach or suggest at least

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two random number generator circuits that produce at least two independent series of random numbers and that continuously provides a series of statistically verified random numbers from the series of random numbers for the random number circuit. As such, the combination of Vasseur I and Vasseur II does not produce a resultant structure that meets the limitations of the present invention, as claimed in Claim 20. Therefore, the rejection under §103 is improper.

In addition, no suggestion can be found in either Vasseur I or Vasseur II to make the combination stated in the rejection. "Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." In re Fritch, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992). In this regard, Vasseur I and Vasseur II, in combination or individually, make no suggestion or indication that the generators produce two independent series of random numbers. Therefore, the combination of Vasseur I and Murata is improper.

Furthermore, since there is not motivation or suggestion to make the combination stated in the rejection, the present rejection is based on impermissible hindsight. The Federal Circuit has stated that "[i]t is impermissible to use the claimed invention as an instruction manual or "template" to piece together teachings of the prior art so that the claimed invention is rendered obvious . . . one cannot use hindsight reconsideration to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." In re Fritch, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992). As such, the rejection under 35 U.S.C. §103 is improper.

Based on these amendments and arguments presented, Claim 20 is not obvious over the combination of Vasseur I over Vasseur II. As such, the rejection under 35 U.S.C. §103 should be withdrawn.

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c. Claims 19 and 35 rejected over Vasseur I

Claims 19 and 35 have been rejected under 35 U.S.C. §103 as being unpatentable over Vasseur I. The rejection states that Vasseur I teaches random number generation and a verification circuit, but Vasseur I does not teach that the random number generator is an ANSI X9.17. The rejection further states that Official Notice is taken the ANSI X9.17 circuits are old and well-known.

In the present invention, Claims 19 and 35 provide a random number generator circuit that comprises an ANSI X9.17 circuit. As stated in the arguments in relation to the §102 rejection based on Vasseur I, the Vasseur I reference does not meet the limitations of independent Claims 17 and 33 because Vasseur I does not teach a random number generator circuit that provides a series of random numbers and that ultimately provide a continuously provides a series of statistically verified random numbers. Based on the dependency of Claims 19 and 35 to independent Claims 17 and 33, the Vasseur I rejection under § 103 is also improper because Vasseur I does not meet the limitations of the claimed invention. Therefore, the rejection of Claims 19 and 35 should be withdrawn.

Further, official notice has been taken that ANSI X9.17 circuits are old and well-known. Should the rejection under §103 be maintained, Applicant respectfully requests that an affidavit be provided, as required by 37 CFR §1.107, that clearly indicates that the ANSI X9.17 is old and well known when taken in conjunction with the present invention as a whole.

d. Claims 21 and 37 rejected over Vasseur I and Murata

Claims 21 and 37 have been rejected under 35 U.S.C. §103 as being unpatentable over Vasseur I in view of Murata as applied to Claims 18 and 36. The rejection states that Vasseur I and Murata teach random number

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generation and a verification circuit that stores the output in a buffer, but the combination does not state that the buffer uses a FIFO system. The rejection further states that Official Notice is taken that FIFO systems are old and well-known.

Claims 21 and 37 provide a buffer that is a first in, first out (FIFO) register. Applicant has set forth the §103 rejection as applied to Claims 18 and 36 above. The arguments and discussion are incorporated in this section. As such, since Vasseur I and Murata do not meet the limitations of Claims 18 and 36 because Vasseur I does not teach a random number generator circuit that produces a series of random numbers and Murata does not teach storage of a continuous series of verified random numbers, the rejection of Claims 21 and 37 is improper.

Further, official notice has been taken that FIFO systems are old and well-known. Should the rejection under §103 be maintained, Applicant respectfully requests that an affidavit be provided, as required by 37 CFR §1.107, that clearly indicates that FIFO systems are old and well-known when taken in conjunction with the present invention as a whole.

e. Claims 22, 38 and 42 rejected over Vasseur I and Murata

Claims 22, 38 and 42 have been rejected under 35 U.S.C. §103 as being unpatentable over Vasseur I in view of Murata as applied to Claims 18 and 36. The rejection states that Vasseur I and Murata teach random number generation and a verification circuit that stores the output in a buffer, but the combination does not disclose that the buffer outputs numbers at a lesser rate than it receives number, nor that the buffer can, for short periods of time, output numbers faster than it receives numbers. The rejection further states that Official Notice is taken that it is old and well-known that a data storage circuit must receive inputs at a rate greater then or equal to the rate of output,

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and Official Notice has been taken that it is old and well-known to allow for data output at a rate faster than data input for a short period of time.

In the present invention, Claims 22, 38 and 42 provide a random number generator circuit where the buffer receives a series of statistically verified random numbers at a first rate. The buffer supplies the series of random numbers at a second rate where the first rate is greater than the second rate. The buffer also provides short term bursts of random numbers where the second rate is greater than the first rate.

Applicant has set forth the §103 rejection as applied to Claims 18 and 36 above. The arguments and discussion are incorporated in this section. As such, since Vasseur I and Murata do not meet the limitations of Claims 18 and 36 because Vasseur I does not teach a random number generator circuit that produces a series of random numbers and Murata does not teach storage of a series of verified random numbers, the rejection of Claims 22, 38 and 42 is improper.

Further, official notice has been taken that it is old and well-known to allow for data output at a rate faster than data input for a short period of time. Should the rejection under §103 be maintained, Applicant respectfully requests that an affidavit be provided, as required by 37 CFR §1.107, that clearly indicates that it is old and well-known to allow for data output at a rate faster than data input for a short period of time when taken in conjunction with the present invention as a whole.

f. Claim 29 rejected over Vasseur I

Claims 29 has been rejected under 35 U.S.C. §103 as being unpatentable over Vasseur I. The rejection states that Vasseur I teaches random number generation and a verification circuit, but Vasseur does not teach that the verification circuit uses an algorithm selected from the set of

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Runs Test, a K-S test, a Chi-square test and a serial test. The rejection further states that Official Notice is taken that the Runs Test, K-S test, Chi-square test and serial test are old and well-known as test to check for randomness.

In the present invention, Claim 29 provides a random number generator circuit that includes a verifier that verifies the random numbers using at least a verification algorithm selected from the set of Runs Test, a K-S test, a Chi-square test and a serial test. As stated in the arguments in relation to the §102 rejection based on Vasseur I, the Vasseur I reference does not meet the limitations of independent Claim 17 because Vasseur I does not teach a random number generator circuit that produces a series of random numbers. Based on the dependency of Claim 29 to independent Claim 17, the Vasseur I rejection under § 103 is also improper because Vasseur I does not meet the limitations of the claimed invention. Therefore, the rejection of Claim 29 should be withdrawn.

Further, official notice has been taken that the Runs Test, K-S test, Chi-square test and serial test are old and well-known as test to check for randomness. Should the rejection under §103 be maintained, Applicant respectfully requests that an affidavit be provided, as required by 37 CFR §1.107, that clearly indicates that the Runs Test, K-S test, Chi-square test and serial test are old and well-known as test to check for randomness when taken in conjunction with the present invention as a whole.

g. Claim 39 rejected over Vasseur I

Claim 39 has been rejected under 35 U.S.C. §103 as being unpatentable over Vasseur I. The rejection states that Vasseur I teaches random number generation and a verification circuit, but Vasseur I does not display an encryption circuit between the random number generation circuit

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and the controller. The rejection further states that Official Notice is taken that encryption of values secures the values from illicit viewers.

In the present invention, Claim 39 provides an encryption circuit connected to the random number generator circuit for encrypting the series of random numbers and providing the encrypted random numbers to the controller. As stated in the arguments in relation to the §102 rejection based on Vasseur I, the Vasseur I reference does not meet the limitations of independent Claim 33 because Vasseur I does not teach a random number generator circuit that produces a series of random numbers. Based on the dependency of Claim 39 to independent Claim 33, the Vasseur I rejection under § 103 is also improper because Vasseur I does not meet the limitations of the claimed invention. Therefore, the rejection of Claim 39 should be withdrawn.

Further, official notice has been taken that encryption of values secures the values from illicit viewers. Should the rejection under §103 be maintained, Applicant respectfully requests that an affidavit be provided, as required by 37 CFR §1.107, that clearly indicates the encryption of values secures the values from illicit viewers and that such encryption is well known when taken in conjunction with the present invention as a whole.

h. Claims 31 and 40 rejected over Vasseur I

Claims 31 and 40 have been rejected under 35 U.S.C. §103 as being unpatentable over Vasseur I. The rejection states that Vasseur I teaches random number generation and a verification circuit, but Vasseur I does not teach about using a DES circuit to produce random numbers. The rejection further states that Official notice is taken that DES circuits are old and well-known and can be used to randomize and secure data and is an approved government standard.

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In the present invention, Claims 31 and 40 provide an encryption circuit that uses a DES circuit. As stated in the arguments in relation to the §102 rejection based on Vasseur I, the Vasseur I reference does not meet the limitations of independent Claims 17 and 33 because Vasseur I does not teach a random number generator circuit that provides a series of random numbers. Based on the dependency of Claims 31 and 40 to independent Claims 17 and 33, the Vasseur I rejection under § 103 is also improper because Vasseur I does not meet the limitations of the claimed invention. Therefore, the rejection of Claims 31 and 40 should be withdrawn.

Further, official notice has been taken that that DES circuits are old and well-known. Should the rejection under §103 be maintained, Applicant respectfully requests that an affidavit be provided, as required by 37 CFR §1.107, that clearly indicates that DES circuits are old and well-known when taken in conjunction with the present invention as a whole.

i. Claims 32 and 41 rejected over Vasseur I

Claims 32 and 41 have been rejected under 35 U.S.C. 103 as being unpatentable over Vasseur I. The rejection states that Vasseur I teaches random number generation and a verification circuit, but Vasseur I does not teach that the encryption uses IDEA encryption. The rejection further states that Official Notice is taken that IDEA encryption is old and well-known in the art of encryption and is fast.

In the present invention, Claims 32 and 41 provide a random number generator circuit that comprises an encryption circuit that includes at least one international data encryption algorithm (IDEA). As stated in the arguments in relation to the §102 rejection based on Vasseur I, the Vasseur I reference

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does not meet the limitations of independent Claims 17 and 33 because Vasseur I does not teach a random number generator circuit that produces a series of random numbers. Based on the dependency of Claims 32 and 41 to independent Claims 17 and 33, the Vasseur I rejection under § 103 is also improper because Vasseur I does not meet the limitations of the claimed invention. Further, the rejection has misstated the present invention as claimed in Claims 32 and 41. In this regard, Claims 32 and 41 use an encryption circuit to produce random numbers and, not to encrypt data, as stated in the rejection. Therefore, the rejection of Claims 32 and 41 should be withdrawn.

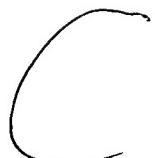
Further, official notice has been taken that IDEA encryption is old and well-known. Should the rejection under §103 be maintained, Applicant respectfully requests that an affidavit be provided, as required by 37 CFR §1.107, that clearly indicates that IDEA encryption is old and well-known when taken in conjunction with the present invention as a whole.

D. Conclusion.

In view of the above amendments and arguments, all of the pending Claims 17-22 and 29-43 are believed to be allowable and the application in condition for allowance which action is requested. If any fees are required, please charge them to the Deposit Account No. 04-1414. Should the Examiner anticipate any action other than allowance of the case, the Examiner is invited to call the below-listed attorney to discuss the case.

Respectfully submitted,

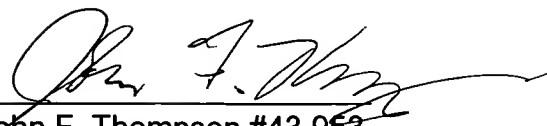
DORR, CARSON, SLOAN & BIRNEY, P.C.



PATENT APPLICATION

Date: 29 Sept. 1999

By



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GP 2767
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Filing Date	October 28, 1997
First Named Inventor	Rolf E. Carlson
Group Art Unit	2767
Examiner Name	D. Meislahn

Attorney Docket Number

1505/5(a)

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